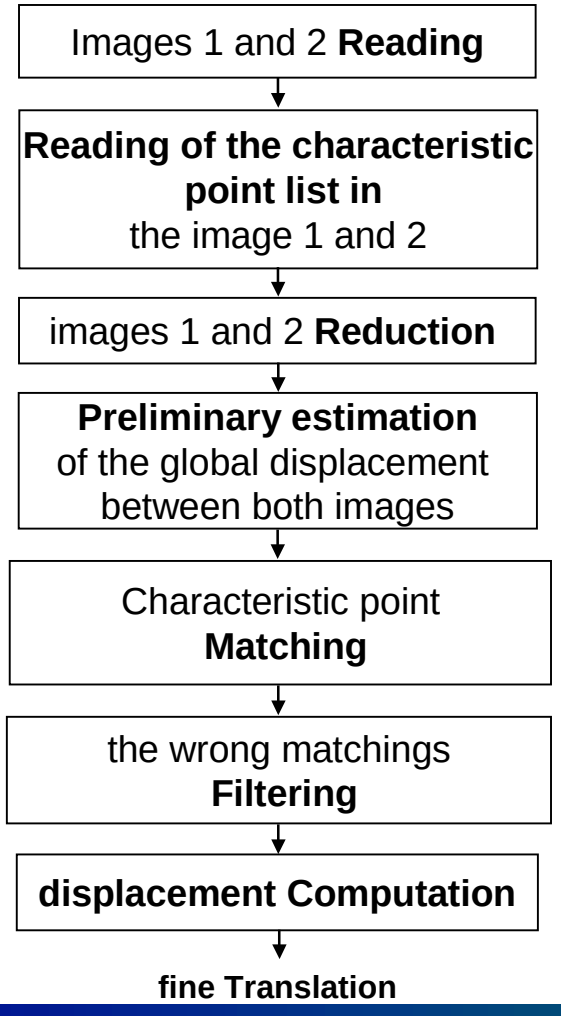
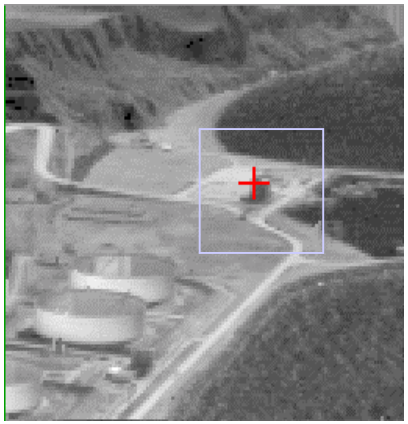
Fast Prototyping of an image processing application with AAA/SynDEx

Control Flow Graph of the application



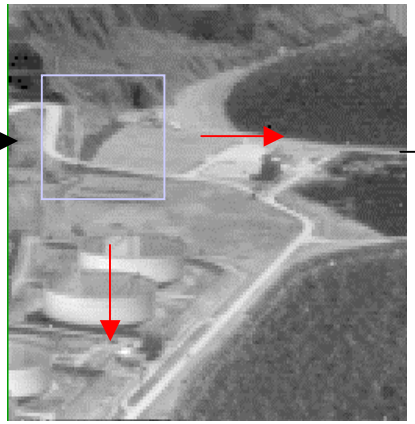
Translation
between 2 images

Interframe Matching and "Greyvalue Corners"



original Frame at t

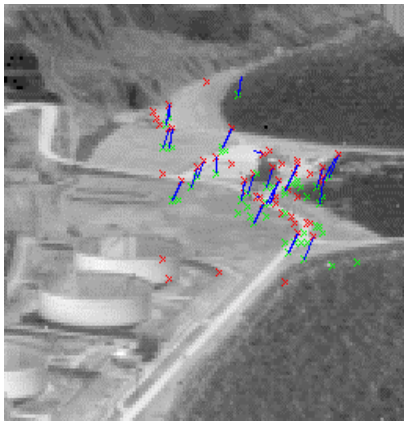
Correlation kernel



Cost(i,j) = ∑ | kernel(k,l) - Frame(k+i,l+j)|
(k,l)∈ kernel

Optimal kernel Position at t+dt

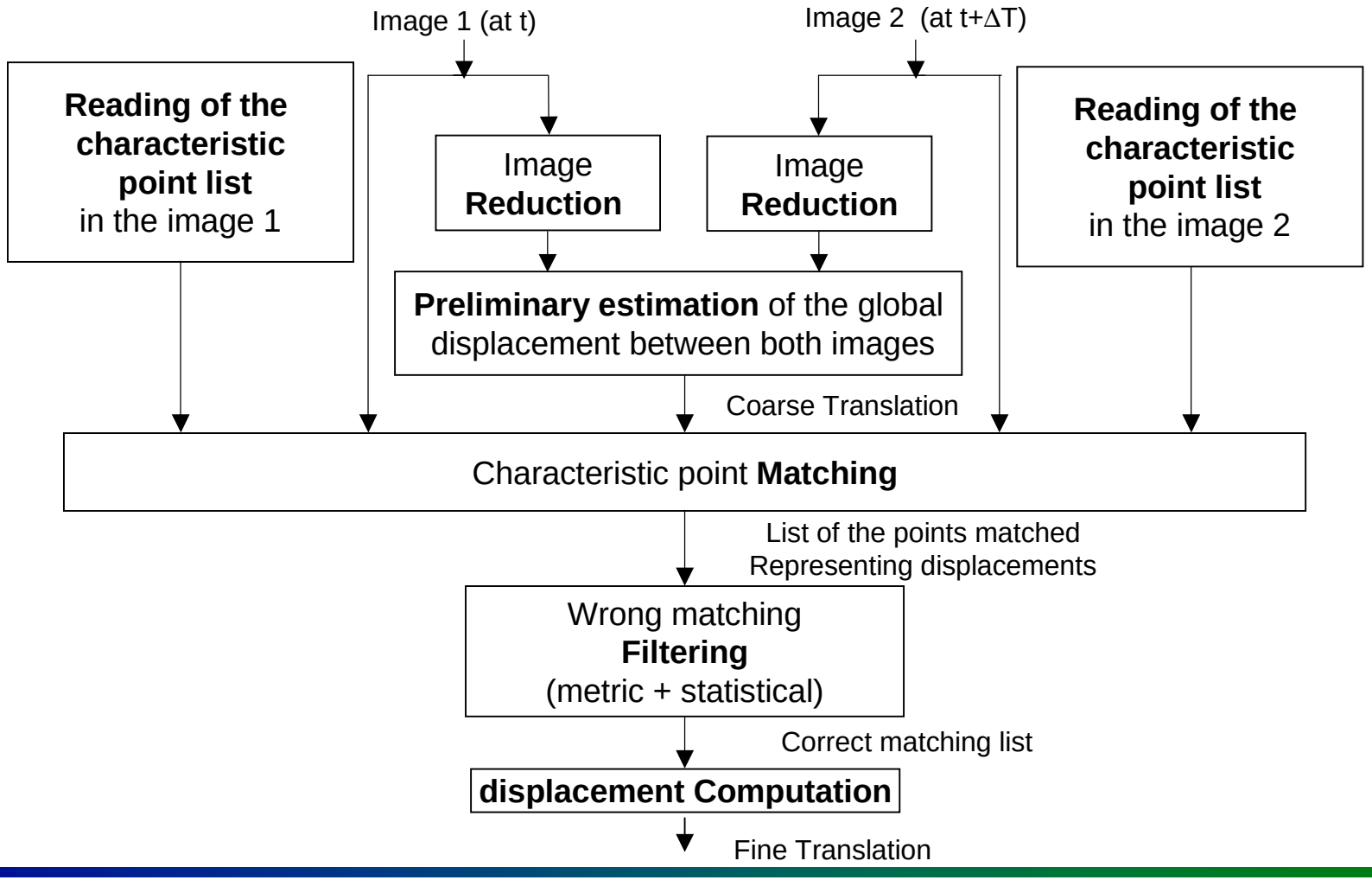
2 successive Frames at t and t+dt



Greyvalue corners matching

New point estimation

First transformation: Operation Parallelism



First Conclusion

- Operation Parallelism
  - **Insufficient to decrease the execution time with 2 processors**
  - **Increasing the Operations Parallelism doesn't solve all the problems**

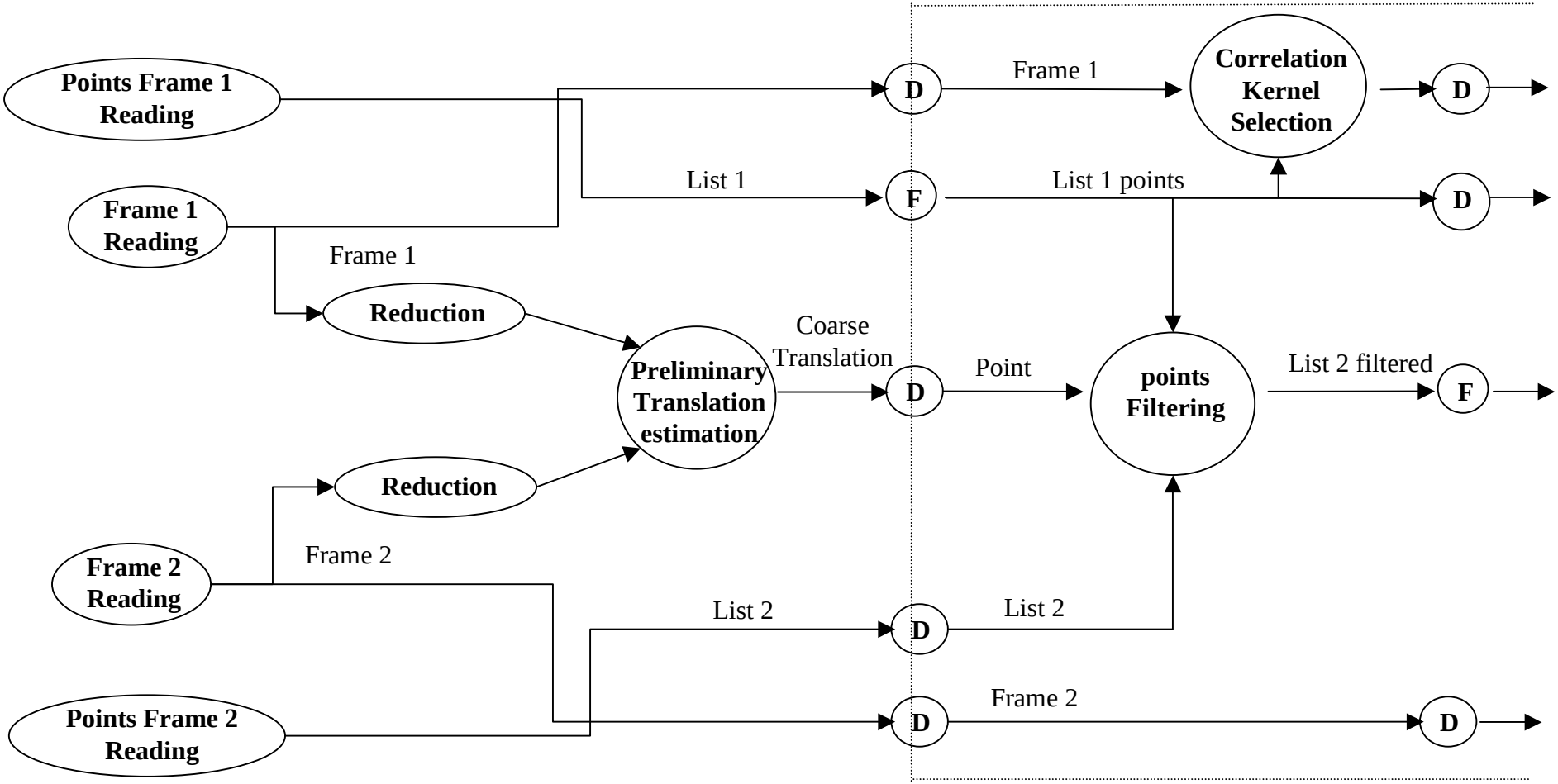
  ↑ **Data Parallelism is required for the algorithm specification**

  ↑ **Also is required:**

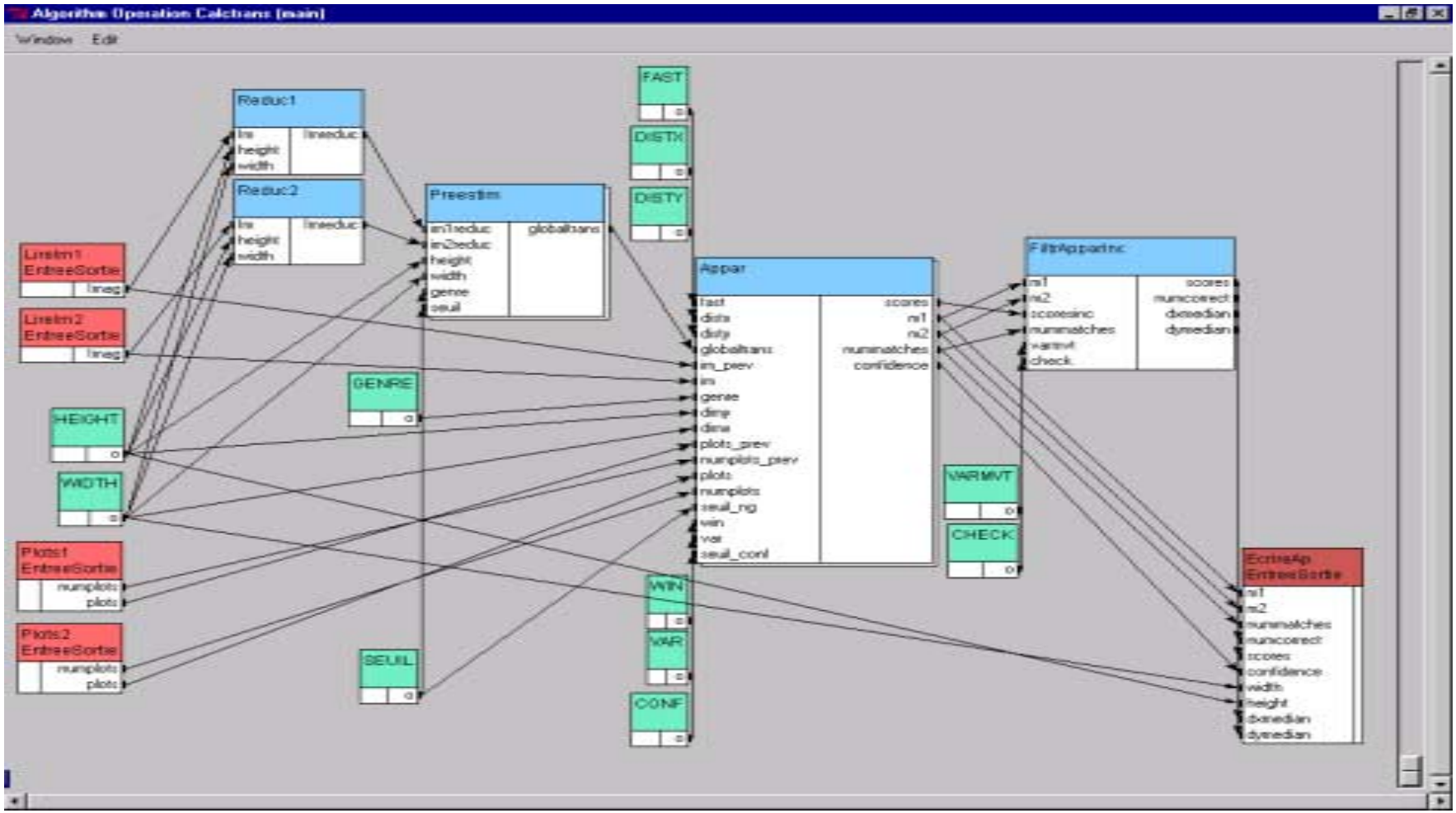
- Hierarchical specification
  - **Simplify specification of complex algorithms**
- Factorization
  - **Specify data parallelism (same operation repeated spatially on different data)**
- Conditioning

  Taken into account by heuristics, when the operations are executed in an exclusive way (never at the same time)

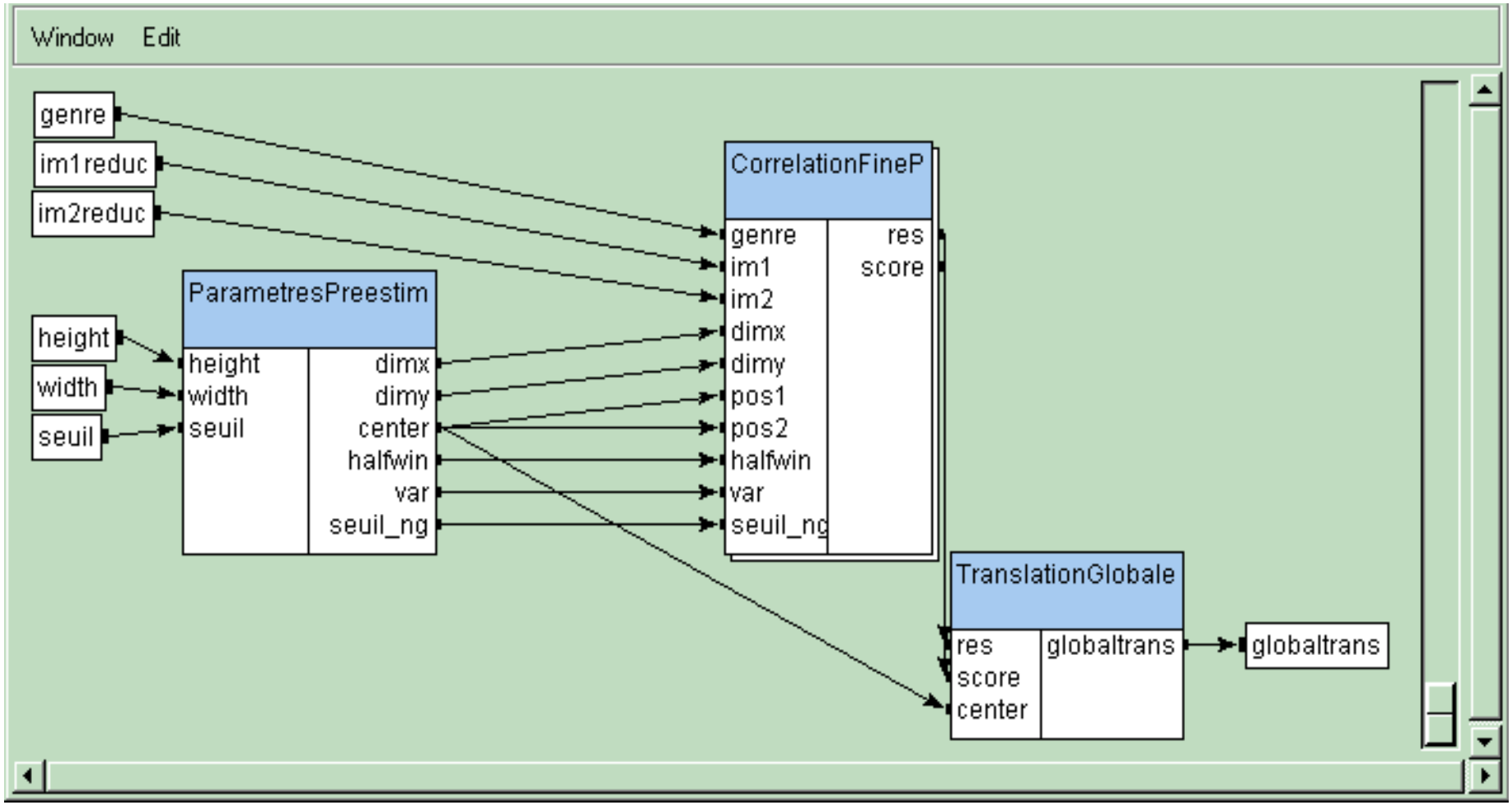
Data Flow Graph of the application (Partial)



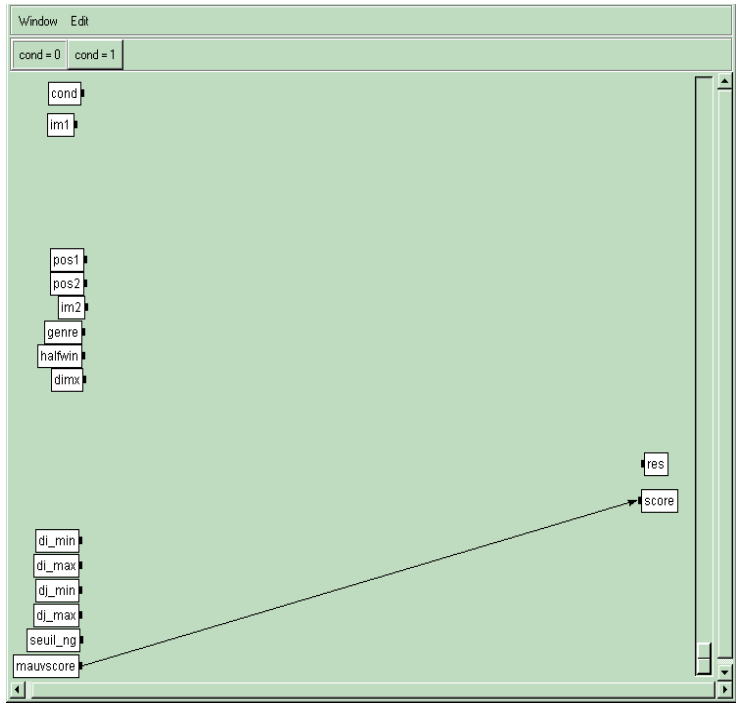
Algorithm Graph of the application with SynDEx

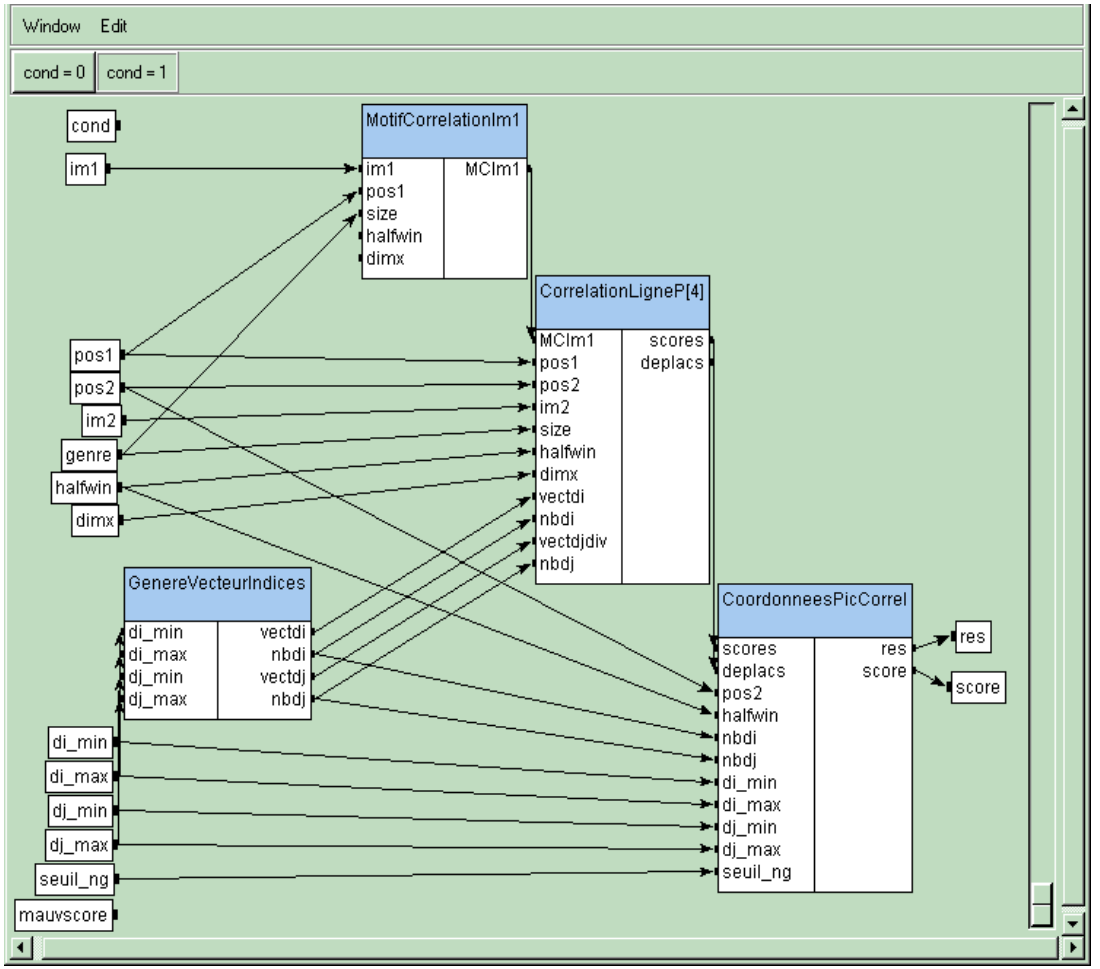


Hierarchical Specification of algorithm "Preestim"



Conditioning specification



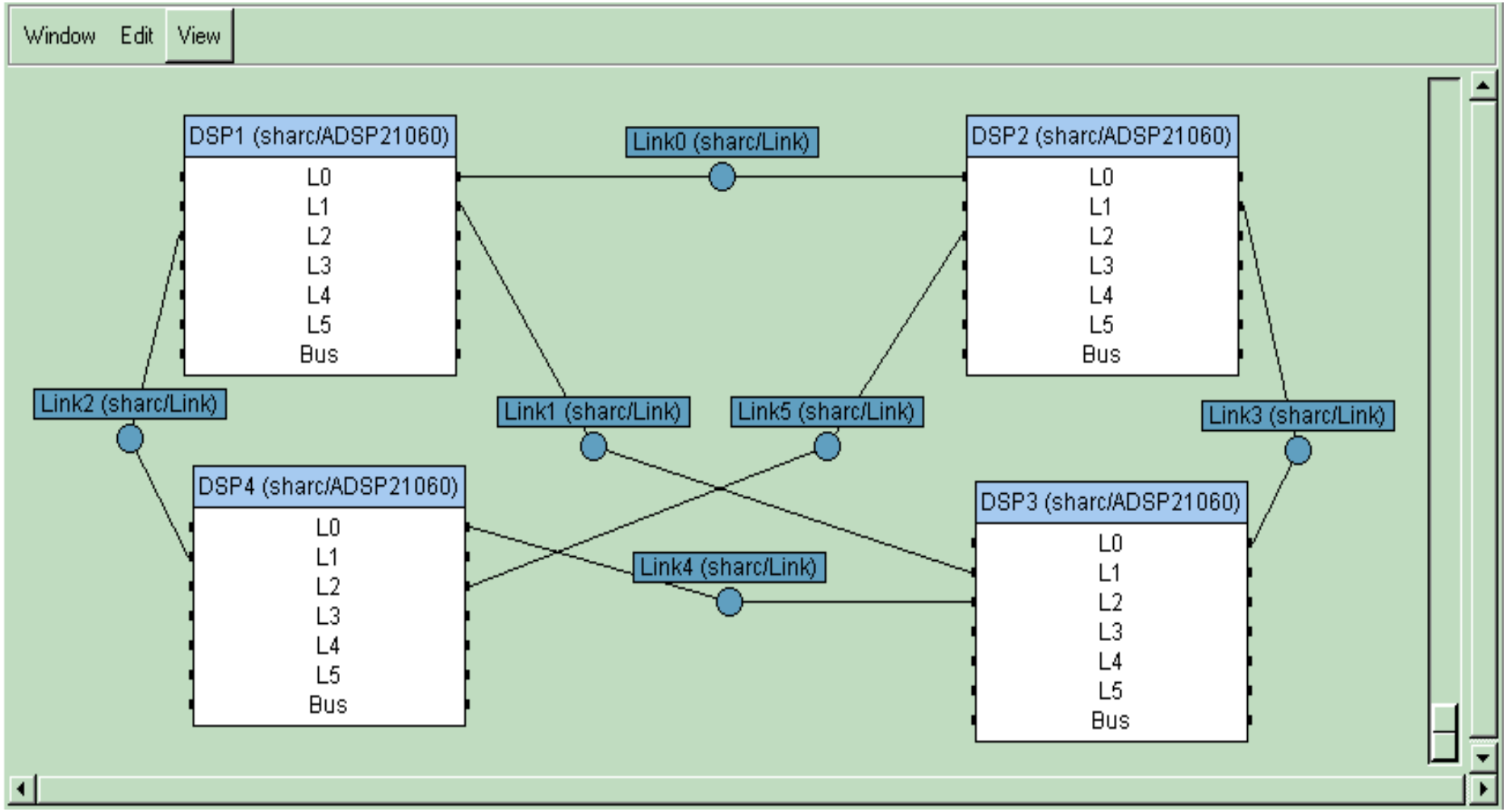


Hardware Graph specifications

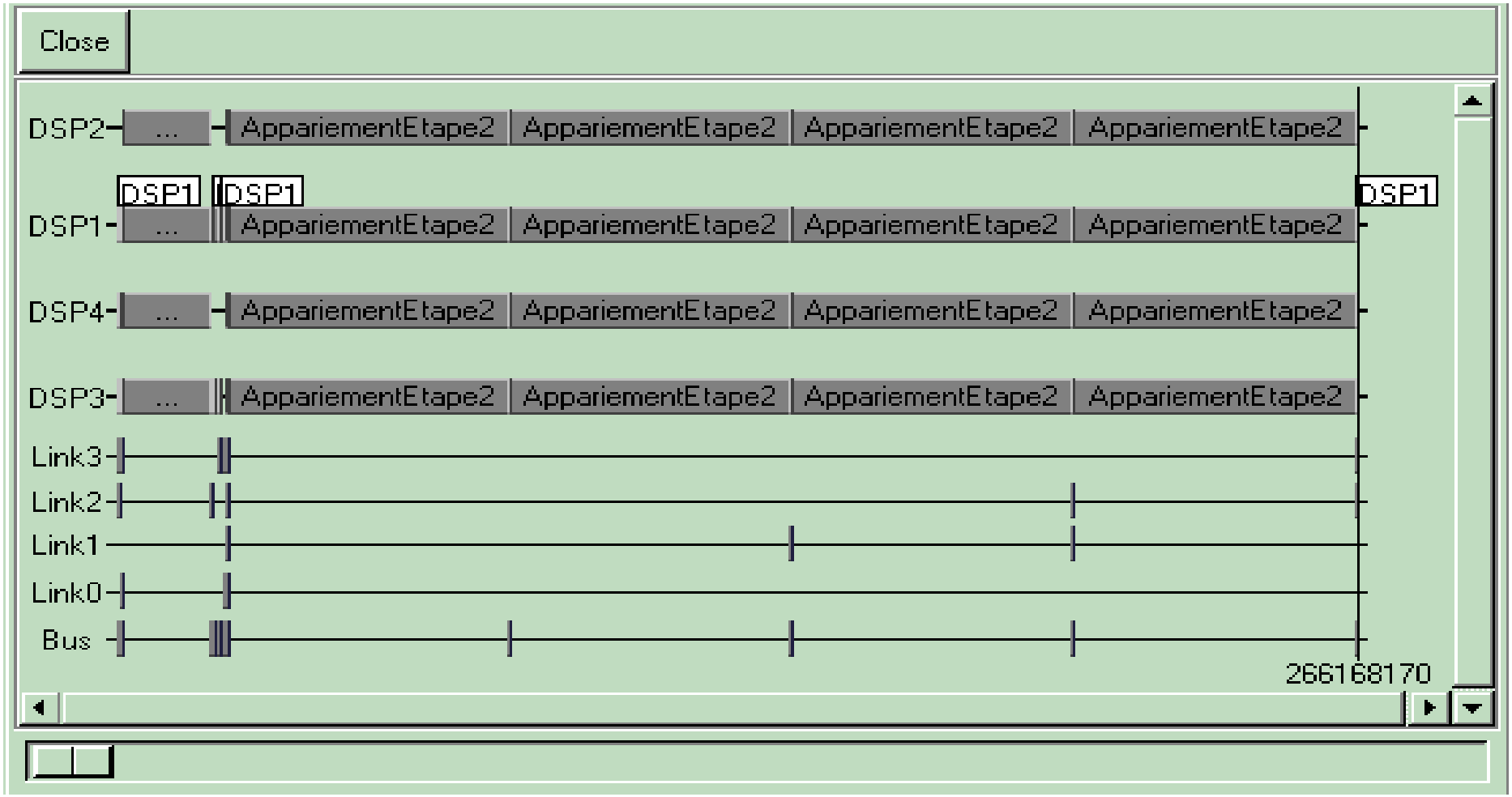
An architecture is defined by the type of used processors
and by the interconnection topology between these processors

- Point to Point in ring (1 to 8 processors tested)
- Completely interconnected (1 to 6 processors tested)
- Point to Point in ring with a common bus (1 to 8 processors tested)

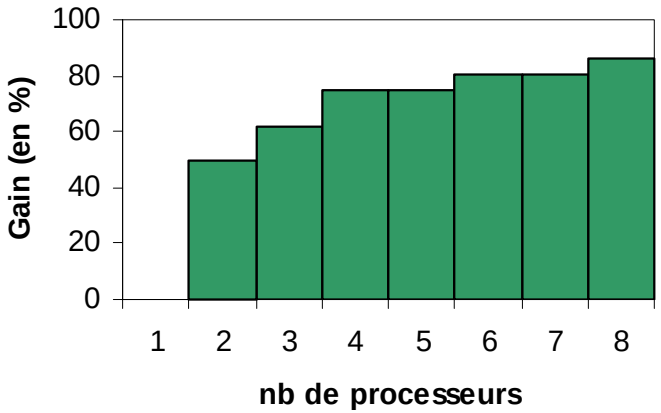
Hardware Graph example



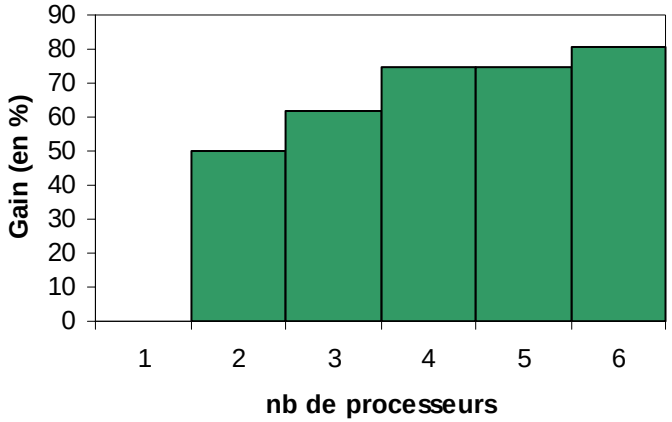
Simulation results for 4 processors



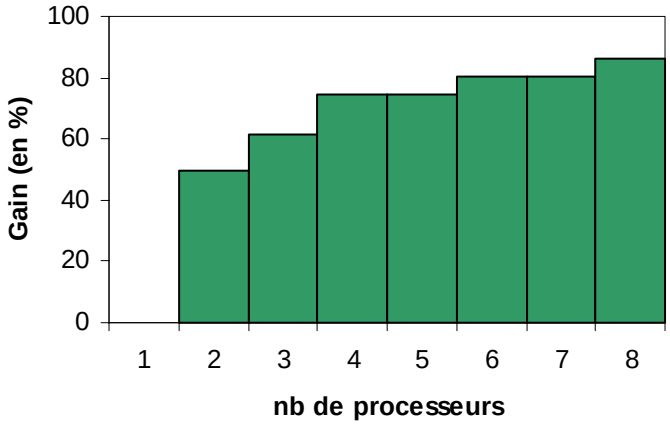
Results



Point to point in ring



Completely Interconnected



Point to point in ring with a common bus